# Microwave Amplifier Design with Potentially Unstable FET's

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*Abstract*—**The concept of maximally efficient gain, as applied to the design of microwave transistor amplifiers with potentially unstable devices, is illustrated by an example, utilizing the parameters of a typical small-signal microwave FET.**

## I. Introduction

THE PRESENCE of internal reverse feedback in microwave transistors often results in devices that are potentially unstable. Such transistors are capable of oscillation without additional feedback and hence do not possess a finite maximum available gain and cannot be simultaneously conjugately matched at both ports. Since a unique set of "best" terminations does not exist from the standpoint of maximum gain, in practice various *ad hoc* design procedures have been developed to determine appropriate terminating impedances.

One common practice is to assume $S_{12}=0$ and to base the design procedure on the resulting unilateral (and fictitious) transistor. This unilateral transistor has a well-defined maximum gain (usually termed the unilateral gain, here denoted by $G_U$) with easily determined optimum terminating impedances. Such a simple first-order design often yields good results. Another approach is to construct gain and stability circles on a Smith chart and exercise design judgment in selecting the desired gain and terminating impedances.

An alternate design approach which yields unique, closed-form solutions for a set of "best" terminating impedances even in the presence of potential instability is one based upon the concept of maximally efficient gain [1]. It is the purpose of this paper to illustrate the application of this technique with a numerical example based upon published $S$-parameter data for a typical small-signal microwave FET.

## II. Theory

The proposed approach avoids the problems associated with infinite gain in potentially unstable devices by selecting terminations which maximize the *difference* between output and input power rather than selecting terminations which maximize the ratio of output power to input power, as is conventionally done. This procedure of maximizing the power difference (or added power) can be viewed as maximizing the activity of the embedded transistor and is identical to the procedure which has been utilized in obtaining a closed-form design procedure for large-signal microwave transistor amplifiers [2]. The power gain which results from this procedure has been termed "maximally efficient gain" ($G_{ME}$). In all cases investigated to date, this gain has remained finite and numerically close to the value obtained for $G_U$. In $y$-parameter notation, the appropriate design expressions are

$$G_{ME}=\frac{|y_{21}/y_{12}|^2-1}{2(k|y_{21}/y_{12}|-1)} \tag{1}$$

$$Y_L=\frac{2g_{22}y_{21}}{y_{21}+y_{12}^*}-y_{22}\cong y_{22}^*, \qquad \text{for } \left|\frac{y_{21}}{y_{12}}\right|\gg 1 \tag{2}$$

$$Y_S=Y_{\text{in}}^*=y_{11}^*-\frac{(y_{21}y_{12})^*-|y_{12}|^2}{2g_{22}} \tag{3}$$

where $k$ is the Rollett stability factor [3], $Y_L$ is the load admittance, $Y_S$ is the source admittance, and $Y_{\text{in}}^*$ is the complex conjugate of the input admittance. For Re $(y_{11})>0$ and Re $(y_{22})>0$, it can be shown that $G_{ME}$ will be finite as long as

$$k>\left|\frac{y_{12}}{y_{21}}\right|=\left|\frac{S_{12}}{S_{21}}\right|.$$

It is unlikely that a practical transistor will violate this condition.

In $S$-parameter notation, the appropriate design expressions are

$$G_{ME}=\frac{|S_{21}/S_{12}|^2-1}{2(k|S_{21}/S_{12}|-1)} \tag{4}$$

$$\Gamma_L\cong\left(S_{22}-\frac{S_{21}S_{12}}{1+S_{11}}\right)^* \tag{5}$$

$$\Gamma_S=\left(S_{11}+\frac{S_{21}S_{12}\Gamma_L}{1-S_{22}\Gamma_L}\right)^*. \tag{6}$$

## III. A Numerical Example

Shown in Table I is a comparison of $G_{ME}$ with the unilateral gain ($G_U$) approximation and the maximum available gain ($G_A$), using published $S$-parameter data for

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TABLE I

| Frequency (GHz) | k | $G_A$ (dB) | $G_U$ (dB) | $G_{ME}$ (dB) | K |
|---|---|---|---|---|---|
| 2.0 | 0.34 | | 22.3 | 20.7 | 5.1 |
| 3.0 | 0.60 | | 17.6 | 16.6 | 7.8 |
| 4.0 | 0.63 | | 15.7 | 15.2 | 7.8 |
| 5.0 | 0.73 | | 13.9 | 13.7 | 8.8 |
| 6.0 | 0.83 | | 12.3 | 12.4 | 9.8 |
| 7.0 | 1.08 | 12.0 | 10.5 | 10.6 | 13.2 |
| 8.0 | 1.22 | 10.4 | 9.3 | 9.5 | 14.1 |
| 9.0 | 1.34 | 9.3 | 8.4 | 8.7 | 14.4 |
| 10.0 | 1.41 | 8.6 | 7.7 | 8.1 | 16.2 |
| 11.0 | 1.53 | 7.9 | 7.1 | 7.5 | 17.4 |
| 12.0 | 1.73 | 6.9 | 6.2 | 6.6 | 19.3 |
| 13.0 | 1.92 | 6.0 | 5.5 | 5.8 | 21.2 |
| 14.0 | 2.12 | 5.2 | 4.7 | 5.0 | 22.7 |

a typical small-signal microwave FET [4]. These data illustrate how $G_{ME}$ can replace both $G_U$ and $G_A$, in effect removing the consideration of potential instability from the design process.

While an amplifier designed by this procedure will be stable as long as $k>|S_{12}/S_{21}|$, from a practical point of view it is also important to assess the *degree* of stability of the resulting amplifier, i.e., to investigate if the required terminations are so close to those which produce instability that they are not viable in an actual amplifier. One figure of merit which has been used to quantify the degree of stability of an amplifier is the overall stability factor $K$ defined by Rollett [3]

$$K=\frac{2(G_S+g_{11})(G_L+g_{22})-\mathrm{Re}\,(y_{21}y_{12})}{y_{21}y_{12}} \tag{7}$$

where $G_S$ is the real part of the source admittance and $G_L$ is the real part of the load admittance. A design is said to be sufficiently stable if the value of $K$ is large compared to unity, with a value of unity representing the point of actual amplifier instability. Table I shows the values of $K$ which are obtained when the $G_{ME}$ approach is used; in every case the overall stability is seen to be quite good.

Stability circles plotted on a Smith chart can also be used to qualitatively assess the degree of stability afforded by a specific set of terminations [5]. An amplifier is considered to be very stable if the locations on the Smith chart which represent the terminations are far removed from the unstable areas delineated by such stability circles. Shown in Fig. 1 are the input and output circuit stability circles for this numerical example evaluated at 4 GHz, together with the locations of the terminations required to yield $G_{ME}$. The points representing the terminations are indeed far removed from the stability circles, again indicating that the overall amplifier so designed is

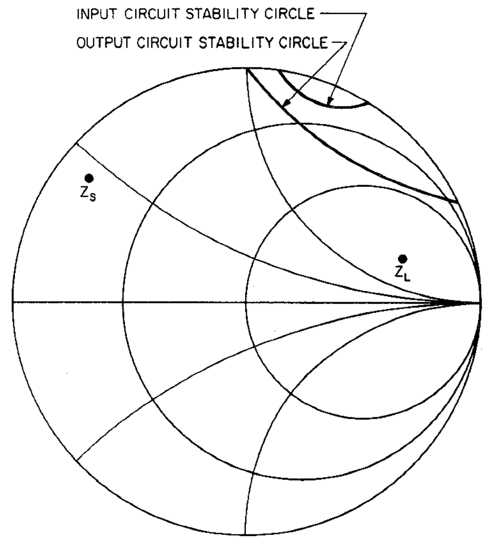


Fig. 1. 4-GHz input and output circuit stability circles, together with the terminations used to give $G_{ME}$.

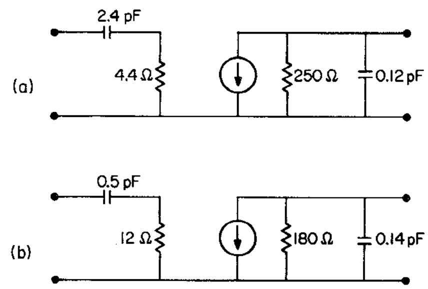


Fig. 2. Two transistor models. (a) Model based upon $G_{ME}$. (b) Model based upon $S_{11}$ and $S_{22}$ alone.

quite stable. From a practical standpoint, this means that moderate errors in the terminations will not lead to instability, nor is it likely that instability will be encountered during the tuning process.

## IV. Transistor Modeling

One current method for the modeling of transistors for the purpose of network synthesis is to use $S_{11}$ alone for the input model and to use $S_{22}$ alone for the output model. This approach has the advantage of simplicity, and it has been shown to be useful in an initial design which can be further refined through the use of computer-aided optimization techniques, utilizing all four $S$ parameters in the final step. An alternate approach would be to use $Y_L^*$ as obtained from (2) as an output model and to use $Y_{\text{in}}$ as obtained from (3) as an input model. In this manner, the effect of the transistor's internal feedback is more accurately modeled, and further computer optimization may not be required.

Fig. 2 shows computed results for the component values of the transistor model using the $G_{ME}$ approach, together with values obtained from $S_{11}$ alone and $S_{22}$ alone. The output models are similar, but a significant difference is seen to exist between the two approaches for modeling the transistor input, showing that the internal feedback is not negligible. Because of this large effect of reverse feedback on the value of the input impedance, more accurate circuit design results should be obtained using the model based upon $G_{ME}$.

## References


[1] K. L. Kotzebue, "Maximally efficient gain: A figure of merit for linear active 2-ports," *Electron. Lett.*, vol. 12, pp. 490–491, Sept. 16, 1976.

[2] ——, "A quasi-linear approach to the design of microwave transistor power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 975–978, Dec. 1976.

[3] J. M. Rollett, "Stability and power-gain invariants of two ports," *IRE Trans. Circuit Theory*, vol. CT-9, pp. 29–32, Mar. 1962.

[4] D. J. Mellor, "Computer-aided synthesis of matching networks for microwave amplifiers," Ph.D. dissertation, Stanford University, Mar. 1975.

[5] G. E. Bodway, "Two-port power flow analysis using generalized scattering parameters," *Microwave J.*, vol. 10, pp. 61–69, May 1967.


# Broad-Band Internal Matching of Microwave Power GaAs MESFET's

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***Abstract*—Broad-band internal matching techniques for high-power GaAs MESFET's at *C* band have been developed, adopting novel circuit configurations and large-signal characterizations in the circuit design. The lumped-element two-section input matching network is formed on a single ceramic plate with a high dielectric constant. The semidistributed single-section output circuit is formed in microstrip pattern on an alumina plate. The internally matched GaAs FET with 11 200-μm total gate width developed has a 2.5-W power output at 1-dB gain compression and a 4.4-W saturated power output with 5.5-dB linear gain from 4.2 to 7.2 GHz without external matching. The FET internally matched from 4.5 to 6.5 GHz exhibited 5-W saturated power output with 6-dB linear gain.**

## I. Introduction

High-power GaAs FET's, exhibiting significant progress in recent years, are realized basically by increasing the total gate width as well as the drain-source breakdown voltage. As a result, the device input impedance decreases steadily in proportion to the total gate width. Thus the maximum attainable power and gain degenerate by matching limitations and losses resulting from the interposition of fixed parasitic elements in the device–circuit interface. To solve such matching limitations and exhibit the basic device capabilities, the introduction of so-called internal matching networks (IMN) close to active device on the carrier or package is a natural consequence. The fixed parasitic elements constrain redundant design, which degrades device broad-band characteristics and brings extra loss.

Internal matching is standard technique for high-power bipolar transistors for use below 5 GHz [1]. With respect to the power GaAs FET of higher frequency capabilities, compared with the bipolar transistors, refined techniques effective at frequencies above 5 GHz are required [2]. In such frequency ranges, input and output phase uniformity within multicell or multichip devices and circuit losses become much more significant.

The purpose of this paper is to present broad-band internal matching techniques for high-power GaAs MESFET's at *C* band [3], adopting novel circuit configurations, where the two-section input matching network is formed on a single thin ceramic plate with a high dielectric constant and large-signal characterizations in the circuit design. The matching circuit losses are also analyzed to obtain a basic understanding of the effect on matching limitations. The internally matched GaAs FET with 11 200-μm total gate width has a 2.5-W power output at 1-dB gain compression and a 4.4-W saturated power output with a linear gain of 5.5 dB from 4.2 to 7.2 GHz without external matching. A 5-W maximum saturated power output has also been measured with narrow-bandwidth design over the 4.5–6.5-GHz frequency range.

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## II. Internal Matching Network Design

For broad-band high-power output performance of power GaAs FET's, large-signal techniques as well as small-signal ones are introduced for the matching network design. In the grounded source configuration, GaAs MESFET optimum power load impedance, by which the maximum power output can be drawn, shifts significantly as a function of input drive level. However, there is little variation in the input impedance. Therefore, large-signal matching is required mainly for the output network, as a first-order consideration.

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